ABSTRACT OF THE DISCLOSURE

A video output controller has a video output buffer, a DMA controller, and a display controller. The display controller has a DMA command list processor configured to determine which of the DMA commands contained in the DMA command list must be issued, an initialize signal port configured to receive an initialize signal for starting initialization, a step signal port configured to receive a step signal for starting the issuance of the DMA command, and an external signal processor configured to provide the DMA command list processor with a timing signal for issuing a DMA command according to the initialize signal and step signal.